Amendments to the Specification

Please replace paragraph [0015] with the following rewritten paragraph:

[0015] The present invention is also directed, according to various embodiments, to a memory cell. Figure 4 illustrates three such memory cells 40. Each memory cell 20 40 may include the magnetic memory element 10 and a transistor 42, such as a field effect transistor (FET). An array of such memory cells 20 40 may form a memory block of a MRAM memory device, as described further herein. The conducting set line 20 (see Figures 1 and 2) may be connected to a terminal of the transistor 42 and pass through the opening of the magnetic memory element 10.

Please replace paragraph [0017] with the following rewritten paragraph:

[0017] The diagrams of Figure 5 help to illustrate the operation of the memory cell 20 40 according to various embodiments of the present invention. Figure 5A shows the magnetization of the reference (or "hard") layer 14. Figure 5B shows a 3D perspective of the magnetic memory element 10. Figures 5C and 5D show magnetic field vectors of the storage ("free") layer 12 for the "1" and "0" states respectively.